Listing of Claims

1. (Currently Amended) An apparatus, comprising:

a semiconductor substrate;

a first conducting layer in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal~~, the base layer metal~~ comprising Cu;

a diffusion barrier in contact with the first conducting layer, wherein the diffusion barrier comprises a metal alloy comprising boron and phosphorus;

a wetting layer on top of the diffusion barrier and comprising one of CoB and NiP; and

a bump layer on top of the wetting layer, the bump layer comprising Sn, wherein the diffusion barrier is configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus.

2. (Previously Presented) The apparatus of Claim 1, wherein the diffusion barrier is configured to suppress whisker-type formation in the bump layer.

3. (Original) The apparatus of Claim 1, further comprising a solder layer positioned between the bump layer and a die package, wherein the solder layer comprises Sn.

4. (Previously Presented) The apparatus of Claim 1, wherein the base layer metal comprises an adhesion layer and a seed layer, wherein the seed layer comprises Co.

5. (Previously Presented) An apparatus, comprising:

a semiconductor substrate;

a first conducting layer in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu;

a diffusion barrier in contact with the first conducting layer, wherein the diffusion barrier comprises a metal alloy comprising boron and phosphorus;

a wetting layer on top of the diffusion barrier; and

a bump layer on top of the wetting layer, the bump layer comprising Sn, wherein the diffusion barrier is configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus,

wherein the base layer metal comprises an adhesion layer and a seed layer, wherein the seed layer comprises Co, wherein the base layer metal further comprises a metal layer positioned between the adhesion layer and the seed layer, wherein the metal layer comprises Al.

6. (Previously Presented) The apparatus of Claim 1, wherein the diffusion barrier comprises NiWBP, wherein the bump layer further comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu, Bi, and Sb, and wherein the bump layer is further configured to prevent low temperature phase transition of Sn from alpha Sn into beta Sn.

7. (Currently Amended) The apparatus of Claim 1, ~~wherein the wetting layer comprises one of CoB and NiP,~~ wherein the diffusion barrier is further configured to reduce bump layer delamination.

8. (Previously Presented) The apparatus of Claim 1, wherein the apparatus further comprises another base layer metal.

9. (Currently Amended) An apparatus comprising:

a base layer metal on a semiconductor substrate, the base layer metal comprising Cu;

a bump on top of the base layer metal, the bump comprising a Cu layer;

a diffusion barrier ~~in contact with~~ on top of the bump, wherein the diffusion barrier comprises a metal alloy comprising boron and phosphorus;

a wetting layer on top of the diffusion barrier; and

a solder layer contacting the ~~bump~~ diffusion barrier, the solder layer comprising Sn, wherein the diffusion barrier is configured to prevent the diffusion of Cu and Sn through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus.

10. (Previously Presented) The apparatus of Claim 9, wherein the diffusion barrier is configured to suppress whisker-type formation in the bump.

11. (Previously Presented) The apparatus of Claim 9, wherein the base layer metal comprises an adhesion layer and a seed layer, wherein the seed layer comprises Co.

12. (Currently Amended) An apparatus comprising:

a base layer metal on a semiconductor substrate, the base layer metal comprising Cu;

a bump on top of the base layer metal, the bump comprising a Cu layer;

a diffusion barrier in contact with the bump, wherein the diffusion barrier comprises a metal alloy comprising boron and phosphorus;

a wetting layer on top of the diffusion barrier; and

a solder layer contacting the ~~bump~~ diffusion barrier, the solder layer comprising Sn, wherein the diffusion barrier is configured to prevent the diffusion of Cu and Sn through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus,

wherein the diffusion barrier is configured to suppress whisker-type formation in the bump, wherein the base layer metal further comprises a metal layer positioned between the adhesion layer and the seed layer, wherein the metal layer comprises Al.

13. (Currently Amended) An apparatus comprising:

a base layer metal on a semiconductor substrate, the base layer metal comprising Cu;

a bump on top of the base layer metal, the bump comprising a Cu layer;

a diffusion barrier ~~in contact with~~ on top of the bump, wherein the diffusion barrier comprises a metal alloy comprising boron and phosphorus;

a wetting layer on top of the diffusion barrier; and

a solder layer ~~on top of~~ in contact with the wetting layer, the solder layer comprising Sn, wherein the diffusion barrier is configured to prevent the diffusion of Cu and Sn through the

diffusion barrier and to prevent CuSn intermetallic formation in the apparatus, and wherein the base layer metal further contacts the diffusion barrier to physically isolate the bump from the solder layer.

14. (Previously Presented) The apparatus of claim 9, wherein the diffusion barrier comprises NiWBP, wherein the wetting layer comprises one of ~~CoB,~~ and NiP.

Claims 15.-31. (Canceled)

32. (Currently Amended) A system having a circuit board, comprising:

one or more components comprising circuitry; and

one or more layers on the circuit board to route at least one signal between components on the circuit board, wherein at least one of the components on the circuit board comprises a die packing interconnect comprising:

a semiconductor substrate;

a first conducting layer in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu;

a diffusion barrier in contact with the first conducting layer, wherein the diffusion barrier comprises a metal alloy comprising boron and phosphorus;

a wetting layer on top of the diffusion barrier and comprising one of CoB and NiP; and

a bump layer on top of the wetting layer, the bump layer comprising Sn, wherein the diffusion barrier is configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the die packing interconnect.

33. (Previously Presented) The system of Claim 32, wherein the one or more components comprise any one of a central processing unit, a memory, and a logic unit, and wherein the diffusion barrier comprises NiWBP.

34. (Previously Presented) The apparatus of Claim 5, wherein the diffusion barrier is configured to suppress whisker-type formation in the bump layer.

35. (Previously Presented) The apparatus of Claim 5, further comprising a solder layer positioned between the bump layer and a die package, wherein the solder layer comprises Sn.

36. (Previously Presented) The apparatus of Claim 5, wherein the diffusion barrier comprises NiWBP, wherein the bump layer further comprises a Sn alloy, the Sn alloy comprising one

of 0.7Cu, Bi, and Sb, and wherein the bump layer is further configured to prevent low temperature phase transition of Sn from alpha Sn into beta Sn.

37. (Previously Presented) The apparatus of Claim 5, wherein the wetting layer comprises one of CoB and NiP, wherein the diffusion barrier is further configured to reduce bump layer delamination.

38. (Previously Presented) The apparatus of Claim 12, wherein the diffusion barrier is configured to suppress whisker-type formation in the bump.

39. (Previously Presented) The apparatus of Claims 9 or 13, wherein the diffusion barrier is configured to suppress whisker-type formation in the bump, wherein the base layer metal further comprises a metal layer positioned between the adhesion layer and the seed layer, wherein the metal layer comprises Al.

40. (Previously Presented) The system of Claim 32, wherein the diffusion barrier is configured to suppress whisker-type formation in the bump, wherein the base layer metal further comprises a metal layer positioned between the adhesion layer and the seed layer, wherein the metal layer comprises Al.

41. (New) A microelectronic device comprising:

a substrate;

a base layer that is connected to circuitry in the substrate, the base layer comprising

a conducting interconnect that includes copper,

an adhesion layer,

a seed layer, and

an aluminum layer between the adhesion layer and the seed layer;

an electroless diffusion barrier comprising any one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP; and

an electroplated bump layer comprising tin,

wherein the electroless diffusion barrier is positioned to prevent intermixing of copper from the base layer and tin from the electroplated bump layer.